IN THE CLAIMS

1 (Currently Amended). A memory comprising:

a first layer and a second layer of memory material spaced from one another in a first direction; and

a first address line and a second address line extending substantially in said first direction through said first and second layers.

2 (Original). The memory of claim 1 wherein said memory material includes a ferroelectric polymer material.

3 (Original). The memory of claim 1 including third and fourth address lines which extend in a second direction different from said first direction.

4 (Original). The memory of claim 3 wherein said first and second directions are substantially transverse to one another.

5 (Original). The memory of claim 3 wherein said third and fourth address lines are in said first layer.

6 (Original). The memory of claim 5 including a first cell formed in said first layer between said first and third address lines and a second cell formed in said first layer between said second and fourth address lines.

7 (Original). The memory of claim 6 wherein a bicell of two cells is formed in said first layer on opposed sides of said third address line.

8 (Original). The memory of claim 7 wherein said bicell is formed between said first and second address lines, and wherein said bicell includes said third address line.

9 (Original). The memory of claim 1 having more than two lines.

10 (Original). The memory of claim 1 having more than two layers.

11 (Original). The memory of claim 1 wherein said layers are vertically stacked.

12 (Original). The memory of claim 11 wherein successive layers are spaced by an insulator.

13 (Original). The memory of claim 1 wherein said lines are vias extending vertically, said memory including a substrate having a surface, said first direction being substantially transverse to said surface.

14 (Withdrawn). A method comprising:

forming a first and a second layer of memory material, said first and second layers spaced in a first direction; and

forming a first and a second address line extending substantially in said first direction through said first and second layers.

15 (Withdrawn). The method of claim 14 including forming a third and fourth address line extending substantially transversely to said first direction.

16 (Withdrawn). The method of claim 15 including forming said third and fourth address lines in said first layer.

17 (Withdrawn). The method of claim 14 including forming a bicell structure.

18 (Withdrawn). The method of claim 14 wherein forming a first and second layer of memory material includes forming ferroelectric polymer memory material layers.

19 (Withdrawn). The method of claim 14 including forming more than two lines and more than two layers.

20 (Withdrawn). The method of claim 14 including forming said lines by forming metal filled vias.

21 (Withdrawn). The method of claim 14 including forming an insulator between said first and second layers.

22 (Withdrawn). A method comprising:

addressing a polymer memory using first lines extending substantially in a first direction to address cells defined in at least two layers spaced from one another in said first direction.

23 (Withdrawn). The method of claim 22 including using second lines extending substantially transversely to said first direction to address cells between said first and second lines.

24 (Withdrawn). The method of claim 23 including addressing a bicell between a second line and two adjacent first lines.

25 (Withdrawn). The method of claim 23 including addressing a cell in one layer by applying a potential to adjacent first and second lines.

26 (Withdrawn). The method of claim 22 wherein addressing includes addressing a ferroelectric polymer memory.

27 (Currently Amended). A system comprising:

a controller;

a wireless interface coupled to said controller; and

a polymer memory coupled to said controller, said memory including a substrate having an upper surface, a plurality of first address lines extending in a first direction, at least two layers of memory material spaced from one another in said first direction, said lines extending through said ~~first and said second layers~~ at least two layers.

28 (Currently Amended). The system of claim 27 including [[a]] third and fourth address ~~line~~ lines extending substantially transversely to the first direction.

29 (Original). The system of claim 28 wherein said lines form a bicell structure.

30 (Original). The system of claim 29 wherein said interface includes a dipole antenna.

31 (Original). The system of claim 27 having more than two lines.

32 (Original). The system of claim 27 wherein said polymer memory is a ferroelectric polymer memory.

33 (Original). The memory of claim 27 having more than two layers.

34 (Original). The memory of claim 27 wherein said layers are vertically stacked.

35 (Original). The memory of claim 34 wherein successive layers are spaced by an insulating layer.

36 (Currently Amended). The memory of claim 27 wherein said lines are vias extending vertically, said substrate having ~~a top~~ an upper surface, said first direction being substantially transverse to said surface.